Amendments to the Claims:

Claim 10 has been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Previously Presented) A device for delivering a clock signal and a digital signal in synchronization to a clocked element of a semiconductor device, comprising:

a phase shift keying circuit for performing phase shift keying of said digital signal onto said clock signal to create a lead output signal and a lag output signal;

a digital signal demodulator for demodulating said lead output signal and said lag output signal from said phase shift keying circuit to retrieve said digital signal; and

a clock signal demodulator for demodulating said lead output signal and said lag output signal in conjunction with said digital signal to retrieve said clock signal.

2. (Original) The device of claim 1, wherein said phase shift keying circuit comprises:

an oscillator for producing a sinusoidal oscillator signal;

a lead phase shift network for receiving said sinusoidal oscillator signal and said digital signal and producing a positive phase shift in said lead output signal when said digital signal has a logical high value; and

a lag phase shift network for receiving said sinusoidal oscillator signal and a complementary digital signal and producing a negative phase shift in said lag output signal when said complementary digital signal has a logical high value.

3. (Original) The device of claim 2, wherein said lead phase shift network comprises a capacitor and a voltage variable resistor forming, in combination, a high pass filter.

4. (Previously Presented) The device of claim 2, wherein said lead phase shift network comprises:

a capacitor having a first terminal for receiving said sinusoidal oscillator signal and a second terminal;

a driver amplifier connected to said second terminal of said capacitor for driving said lead output signal; and

an NMOS transistor configured as a voltage variable resistor having a drain connected to said digital signal for controlling a resistance of said NMOS transistor, said NMOS transistor being connected between said capacitor and said driver amplifier.

5. (Original) The device of claim 2, wherein said lag phase shift network comprises a voltage variable resistor and a capacitor forming, in combination, a low pass filter.

6. (Previously Presented) The device of claim 2, wherein said lag phase shift network comprises:

an NMOS transistor configured as a voltage variable resistor having a drain connected to said complementary digital signal for controlling a resistance of said NMOS transistor and for receiving said sinusoidal oscillator signal;

a driver amplifier connected to said NMOS transistor for driving said lag output signal; and

a capacitor connected between said NMOS transistor and said driver amplifier.

7. (Previously Presented) The device of claim 2, wherein said lead output signal comprises a voltage represented by the function $V_x = A \sin(\omega t + \phi)$ when said digital signal has a logical high value and a voltage represented by the function $V_x = A \sin(\omega t)$ when said digital signal has a logical low value, wherein A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift.

8. (Original) The device of claim 2, wherein said lag output signal comprises a voltage represented by the function $V_{\bar{x}} = A \sin(\omega t - \phi)$ when said complementary digital signal has a logical high value and a voltage represented by the function $V_{\bar{x}} = A \sin(\omega t)$ when said complementary digital signal has a logical low value, wherein A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift.

9. (Original) The device of claim 2, wherein said phase shift in said lead output signal and said lag output signal are of equal magnitude but having opposite signs.

10. (currently amended) The device of claim 1, wherein said digital signal demodulator comprises:

a differential amplifier for comparing said lead output signal and said lag output signal to produce a differential output signal;

a transistor amplifier circuit for receiving said differential output signal and producing a transistor signal dependent upon the square of an AC component of said differential output signal;

an RC low pass filter for receiving said transistor signal and outputting a voltage signal; and

a voltage comparing circuit for receiving said voltage signal and a voltage reference signal to produce ~~a demodulated digital data~~ said digital signal.

11. (Original) The device of claim 10, wherein said differential amplifier comprises a differential amplifier for producing a differential output signal having a voltage represented by the function $V = 2\ V_T + 2\ A \cos(\omega t)\sin(\phi)$ when said lead output signal and said lag output signal are phase shifted, wherein V_T is a threshold voltage of a set of transistors in said transistor amplifier circuit, A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift in said lead output signal and said lag output signal.

12. (Previously Presented) The device of claim 10, wherein said transistor amplifier circuit comprises:

a PMOS load transistor having a PMOS source, a PMOS gate connected to said PMOS source, and a PMOS drain connected to a power supply voltage; and

an NMOS transistor having a gate connected to said differential output signal, a source connected to ground, and a drain connected to said PMOS source and said PMOS gate, wherein said PMOS load transistor and said NMOS transistor produce said transistor signal dependent upon the square of an AC component of said differential output signal.

13. (Original) The device of claim 12, wherein said power supply voltage is four times a threshold voltage of said PMOS load transistor and said NMOS transistor.

14. (Original) The device of claim 12, wherein said transistor amplifier circuit comprises a transistor amplifier circuit for producing said transistor signal having a voltage represented by the function $V = 2V_T - 2\ A\cos(\omega t)\sin(\phi) - [4A^2 / (4V_T)]\cos^2(\omega t)\sin^2(\phi)$ when said lead output signal and said lag output signal are phase shifted, wherein V_T is a threshold voltage of said PMOS load transistor and said NMOS transistor, A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift in said lead output signal and said lag output signal.

15. (Original) The device of claim 10, wherein said RC low pass filter comprises a resistor and a capacitor configured, in combination, to convert said transistor signal to said voltage signal having a voltage $V = 2\ V_T - \frac{1}{2}\ [(4A^2 / (4V_T))\sin^2(\phi)]$, wherein V_T is a threshold voltage of a set of transistors in said transistor amplifier circuit, A is an arbitrary constant, and ϕ is the amount of phase shift in said lead output signal and said lag output signal.

16. (Previously Presented) The device of claim 1, wherein said clock signal demodulator comprises:

a lag phase shift network for receiving said lead output signal and removing a positive phase shift of said lead output signal to recover a first clock signal;

a lead phase shift network for receiving said lag output signal and adding a negative phase shift

of said lag output signal to recover a second clock signal; and

an analog adder for receiving said first clock signal and said second clock signal and averaging said first clock signal and said second clock signal and reducing noise thereon to produce said clock signal.

17. (Original) The device of claim 16, wherein said lag phase shift network comprises a low pass filter including a voltage variable resistor and a capacitor.

18. (Previously Presented) The device of claim 16, wherein said lag phase shift network further comprises:

an NMOS transistor configured as a voltage variable resistor having a drain connected to a first voltage source for controlling a resistance of said NMOS transistor and for receiving said lead output signal;

a driver amplifier connected to said NMOS transistor for driving said first clock signal; and

a capacitor connected between said NMOS transistor and said driver amplifier.

19. (Original) The device of claim 18, wherein said first voltage source comprises a voltage V represented by the equation:

$V = V_{DC} - BV_D$

where V_{DC} is a constant DC voltage, B is an arbitrary constant, and V_D is said digital signal from said digital signal demodulator.

20. (Original) The device of claim 16, wherein said lead phase shift network comprises a high pass filter including a capacitor and a voltage variable resistor.

21. (Previously Presented) The device of claim 16, wherein said lead phase shift network further comprises:

a capacitor having a first terminal for receiving said lag output signal and a second terminal;

a driver amplifier connected to said second terminal of said capacitor for driving said second clock signal; and

an NMOS transistor configured as a voltage variable resistor having a drain connected to a second voltage source for controlling a resistance of said NMOS transistor, said NMOS transistor connected between said capacitor and said driver amplifier.

22. (Original) The device of claim 21, wherein said second voltage source comprises a voltage V represented by the equation:

$V = V_{DC} + BV_D$

where V_{DC} is a constant DC voltage, B is an arbitrary constant, and V_D is said digital signal from said digital signal demodulator.

23. (Original) The device of claim 16, wherein said analog adder comprises:

a set of resistors for reducing noise on said first clock signal and said second clock signal; and

an amplifier in combination with a resistor for receiving said first clock signal and said second clock signal to average and produce said clock signal.

24. (Previously Presented) A device for performing phase shift keying of a digital signal, comprising:

an oscillator for producing a sinusoidal oscillator signal;

a lead phase shift network receiving said sinusoidal oscillator signal and said digital signal for producing a positive phase shift in a lead output signal when said digital signal has a logical high value; and

a lag phase shift network receiving said sinusoidal oscillator signal and a complementary digital signal for producing a negative phase shift in a lag output signal when said complementary digital signal has a logical high value.

25. (Original) The device of claim 24, wherein said lead phase shift network

comprises a capacitor and a voltage variable resistor forming, in combination, a high pass filter.

26. (Original) The device of claim 24, wherein said lead phase shift network comprises:

a capacitor having a first terminal for receiving said sinusoidal oscillator signal and a second terminal;

a driver amplifier connected to said second terminal of said capacitor for driving said lead output signal of said lead phase shift network; and

an NMOS transistor configured as a voltage variable resistor having a drain connected to said digital signal for controlling a resistance of said NMOS transistor, said NMOS transistor connected between said capacitor and said driver amplifier.

27. (Original) The device of claim 24, wherein said lag phase shift network comprises a voltage variable resistor and a capacitor forming, in combination, a low pass filter.

28. (Original) The device of claim 24, wherein said lag phase shift network comprises:

an NMOS transistor configured as a voltage variable resistor having a drain connected to said complementary digital signal for controlling a resistance of said NMOS transistor and for receiving said sinusoidal oscillator signal;

a driver amplifier connected to said NMOS transistor for driving said lag output signal of said lag phase shift network; and

a capacitor connected between said NMOS transistor and said driver amplifier.

29. (Original) The device of claim 24, wherein said lead output signal from said lead phase shift network comprises a voltage represented by the function $V_x = A \sin(\omega t + \phi)$ when said digital signal has a logical high value and a voltage represented by the function $V_x = A \sin(\omega t)$ when said digital signal has a logical low value, wherein A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift.

30. (Original) The device of claim 24, wherein said lag output signal from said lag phase shift network comprises a voltage represented by the function $V_{\bar{x}} = A \sin(\omega t - \phi)$ when said complementary digital signal has a logical high value and a voltage represented by the function $V_{\bar{x}} = A \sin(\omega t)$ when said complementary digital signal has a logical low value, wherein A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift.

31. (Original) The device of claim 24, wherein said phase shift in said lead output signal and said lag output signal are of equal magnitude but having opposite signs.

32. (Previously Presented) A device for demodulating a phase shift keyed signal from a lead signal and a lag signal, comprising:

a differential amplifier for comparing said lead signal and said lag signal to produce a differential output signal;

a transistor amplifier circuit for receiving said differential output signal and producing a transistor signal dependent upon the square of an AC component of said differential output signal;

an RC low pass filter for receiving said transistor signal and outputting a voltage signal;

a voltage comparing circuit for receiving said voltage signal and a voltage reference signal to produce a demodulated digital data signal.

33. (Original) The device of claim 32, wherein said differential amplifier comprises a differential amplifier for producing a differential output signal having a voltage represented by the function $V = 2 V_T + 2 A \cos(\omega t)\sin(\phi)$ when said lead signal and said lag signal are phase shifted, wherein V_T is a threshold voltage of a set of transistors in said transistor amplifier circuit, A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift in said lead signal and said lag signal.

34. (Previously Presented) The device of claim 32, wherein said transistor amplifier circuit comprises:

a PMOS load transistor having a PMOS source, a PMOS gate connected to said PMOS source, and a PMOS drain connected to a power supply voltage; and

an NMOS transistor having a gate connected to said differential output signal, a source connected to ground, and a drain connected to said PMOS source and said PMOS gate, wherein said PMOS load transistor and said NMOS transistor produce said transistor signal dependent upon the square of an AC component of said differential output signal.

35. (Original) The device of claim 34, wherein said power supply voltage is four times a threshold voltage of said PMOS load transistor and said NMOS transistor.

36. (Original) The device of claim 34, wherein said transistor amplifier circuit comprises a transistor amplifier circuit for producing said transistor signal having a voltage represented by the function $V = 2V_T - 2\ A \cos(\omega t)\sin(\phi) - [4A^2 / (4V_T)] \cos^2(\omega t)\sin^2(\phi)$ when said lead signal and said lag signal are phase shifted, wherein V_T is a threshold voltage of said PMOS load transistor and said NMOS transistor, A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift in said lead signal and said lag signal.

37. (Original) The device of claim 32, wherein said RC low pass filter comprises a resistor and a capacitor configured, in combination, to convert said transistor signal to said voltage signal having a voltage $V = 2\ V_T - \frac{1}{2} [(4A^2 / (4V_T))\sin^2(\phi)]$, wherein V_T is a threshold voltage of a set of transistors in said transistor amplifier circuit, A is an arbitrary constant, and ϕ is the amount of phase shift in said lead signal and said lag signal.

38. (Previously Presented) A method of synchronizing clock signals and digital data signals on an integrated circuit chip, comprising:

generating a sinusoidal oscillator signal, a digital signal and a complementary digital signal;

creating a lead output signal from said sinusoidal oscillator signal and said digital signal;

creating a lag output signal from said sinusoidal oscillator signal and said complementary digital signal;

transmitting said lead output signal and said lag output signal on matched interconnection lines to a vicinity of a clocked element;

demodulating said lead output signal and said lag output signal for retrieving said digital signal;

demodulating said lead output signal and said lag output signal using said digital signal for retrieving a clock signal; and

inputting said digital signal and said clock signal into said clocked element.

39. (Previously Presented) The method of claim 38, wherein said creating a lead output signal comprises creating a lead output signal having a positive phase shift when said digital signal has a logical high value.

40. (Previously Presented) The method of claim 38, wherein said creating a lead output signal comprises creating a voltage signal V_x represented by the function $V_x = A \sin(\omega t + \phi)$ when said digital signal has a logical high value and creating a voltage signal V_x represented by the function $V_x = A \sin(\omega t)$ when said digital signal has a logical low value, wherein A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift.

41. (Previously Presented) The method of claim 38, wherein creating said lag output signal comprises creating a lag output signal having a negative phase shift when said complementary digital signal has a logical high value.

42. (Original) The method of claim 38, wherein creating said lag output signal comprises creating a voltage signal $V_{\bar{x}}$ represented by the function $V_{\bar{x}} = A \sin(\omega t - \phi)$ when said complementary digital signal has a logical high value and creating a voltage signal $V_{\bar{x}}$ represented by the function $V_{\bar{x}} = A \sin(\omega t)$ when said complementary digital signal has a logical low value, wherein A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount

of phase shift.

43. (Previously Presented) The method of claim 38, wherein creating said lead output signal and said lag output signal comprises:

creating a lead output signal having a positive phase shift ϕ; and

creating a lag output signal having a negative phase shift ϕ, wherein said positive phase shift ϕ and said negative phase shift ϕ are of equal magnitude.

44. (Original) The method of claim 38, wherein demodulating said lead output signal and said lag output signal for retrieving said digital signal comprises:

comparing said lead output signal and said lag output signal for producing a differential output signal;

producing a signal dependent upon the square of an AC component of said differential output signal for creating a voltage signal; and

comparing said voltage signal and a voltage reference signal for producing said digital signal.

45. (Original) The method of claim 44, further comprising producing a differential output signal having a voltage represented by the function $V = 2\ V_T + 2\ A\ \cos(\omega t)\sin(\phi)$ when said lead output signal and said lag output signal are phase shifted, wherein V_T is a threshold voltage, A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift in said lead output signal and said lag output signal.

46. (Previously Presented) The method of claim 44, wherein said producing a signal dependent upon the square of an AC component of said differential output signal comprises producing a signal having a voltage represented by the function $V = 2V_T - 2\ A\ \cos(\omega t)\sin(\phi) - [4A^2 / (4V_T)]\ \cos^2(\omega t)\sin^2(\phi)$ when said lead output signal and said lag output signal are phase shifted, wherein V_T is a threshold voltage, A is an arbitrary constant, ω is the oscillator frequency, and ϕ is the amount of phase shift in said lead output signal and said lag output signal.

47. (Original) The method of claim 44, further comprising creating a voltage signal having a voltage $V = 2\ V_T - \frac{1}{2}\ [(4A^2 / (4V_T))\sin^2(\phi)]$ from said signal, wherein V_T is a threshold voltage, A is an arbitrary constant, and ϕ is the amount of phase shift in said lead output signal and said lag output signal.

48. (Original) The method of claim 38, wherein demodulating said lead output signal and said lag output signal knowing said digital signal for retrieving said clock signal comprises:
removing a positive phase shift from said lead output signal for producing a first clock signal;
removing a negative phase shift from said lag output signal for producing a second clock signal; and
averaging said first clock signal and said second clock signal for retrieving said clock signal.